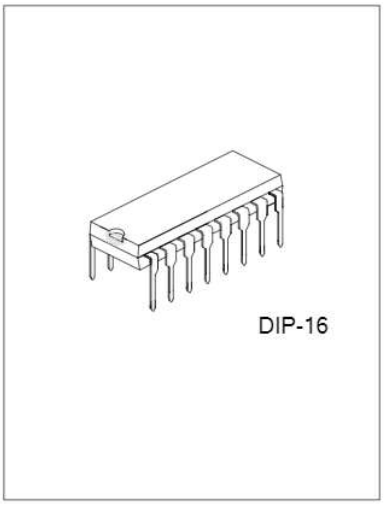
TEA2025

LINEAR INTEGRATED CIRCUIT

STEREO AUDIO AMPLIFIER



■ DESCRIPTION

The UTC TEA2025 is a monolithic integrated audio amplifier in a 16-pin plastic dual in line package. It is designed for portable cassette players and radios.

■ FEATURES

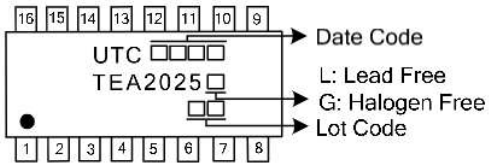
*Working Voltage down to 3V
*Few External components
*High Channel isolation
*Voltage gain up to 45dB(Adjustable with external resistor)
*Soft clipping
*Internal Thermal protection

■ ORDERING INFORMATION

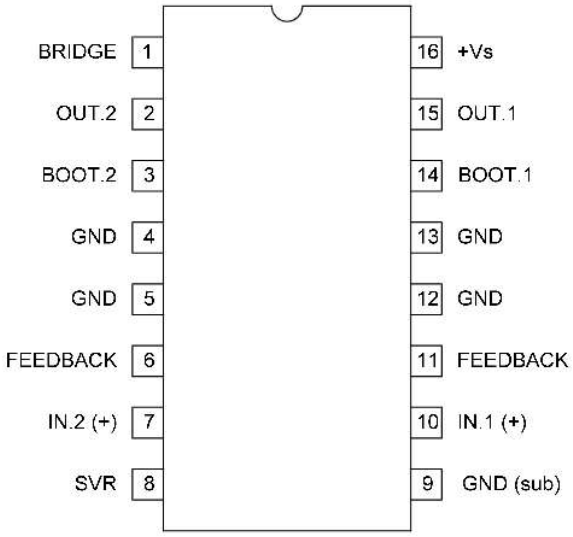
Order Number		Package	Packing
Lead Free	Halogen Free		
TEA2025L-D16-T	TEA2025G-D16-T	DIP-16	Tube

TEA2025L-D16-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube (2) D16: DIP-16 (3) L: Lead Free, G: Halogen Free and Lead Free

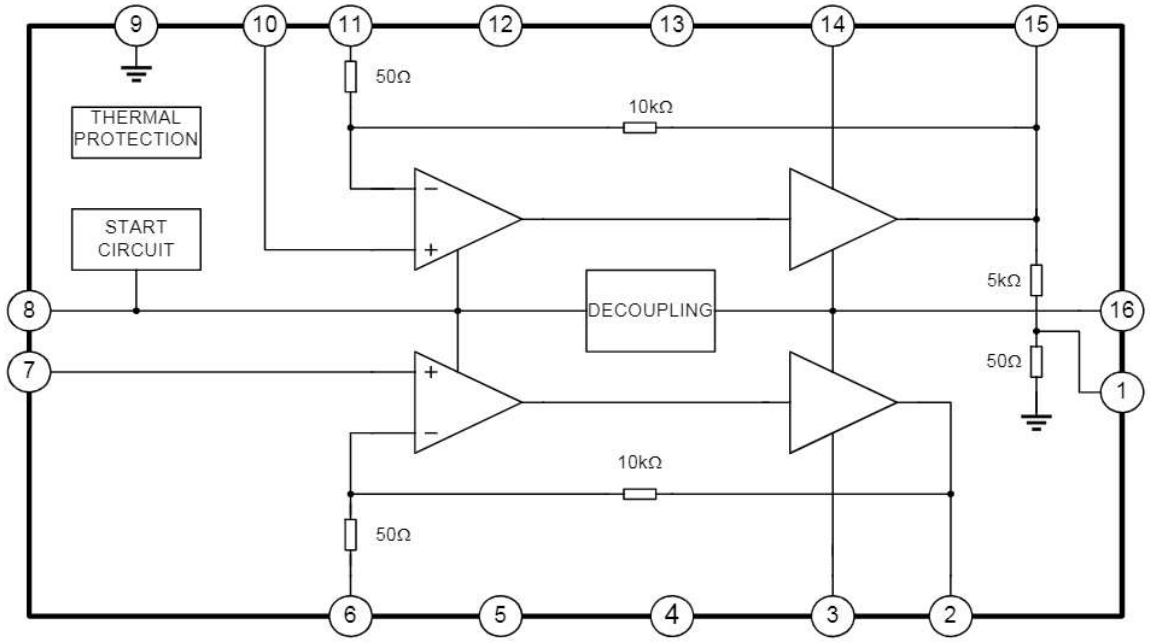
■ MARKING



■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{SS}	15	V
Peak Output Current	$I_{O\ (peak)}$	1.5	A
Junction Temperature	T_J	150	°C
Operating Temperature	T_{OPR}	-20 ~ +85	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The device is guaranteed to meet performance specification within 0°C ~70°C operating temperature range and assured by design from –20°C ~85°C.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Thermal Resistance Junction to ambient	θ_{JA}	60	°C/W
Thermal Resistance Junction to case	θ_{JC}	15	°C/W

■ ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC}=9V, Stereo, unless otherwise specified.)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{SS}		3		12	V
Quiescent Current		I_Q			40	50	mA
Quiescent Output Voltage		V_{OUT}			4.5		V
Voltage Gain		G_V	Stereo	43	45	47	dB
			Bridge	49	51	53	
Voltage Gain Difference		ΔG_V				+-1	dB
Input Impedance		R_{IN}			30		kΩ
Output Power	R_L=4Ω	P_{OUT}	f=1kHz,THD=10%, V_{CC}=9V Stereo per channel	1.7	2.3		W
	R_L=8Ω				1.3		
	R_L=4Ω		V_{CC}=6V	0.7	1		
	R_L=8Ω				0.6		
	R_L=4Ω		V_{CC}=3V		0.1		
	R_L=8Ω		Bridge, V_{CC}=9V		4.7		
	R_L=4Ω		V_{CC}=6V		2.8		
Total Harmonic Distortion	Stereo	THD	V_{CC}=9V, R_L=4Ω, f=1kHz,P_{OUT}=250mW		0.3	1.5	%
	Bridge				0.5		
Supply Voltage Rejection		SVR	R_G=0,AV=45Db,V_{RIPPLE}=150mV F_{RIPPLE}=100Hz	40	46		dB
Input Noise Voltage	R_G=0	Vn	A_V=200, Bandwidth:20Hz ~ 20kHz		1.5	3	μV
	R_G=10kΩ				3	6	
Cross-Talk		C.T.	R_G=10kΩ, f=1kHz,R_L=4Ω, P_{OUT}=1W	40	55		dB

■ APPLICATION INFORMATION

Input Capacitor

Input capacitor is PNP type allowing source to be referenced to ground. In this way no input coupling capacitor is required. However, a series capacitor (0.22 uF)to the input side can be useful in case of noise due to variable resistor contact.

Bootstrap

The bootstrap connection allows to increase the output swing. The suggested value for the bootstrap capacitors (100uF) avoids a reduction of the output signal also at low frequencies and low supply voltages.

Voltage Gain Adjust

STEREO MODE （Figure 1）

The voltage gain is determined by on-chip resistors R1 and R2 together with the external RfC1 series connected between pin 6 (11) and ground. The frequency response is given approximated by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1}{R_f + R_2 + \frac{1}{JWC1}}$$

With R_f=0, C_1=100μF, the gain results 46 dB with pole at f=32 Hz.

THE purpose of Rf is to reduce the gain. It is recommended to not reduce it under 36 dB.

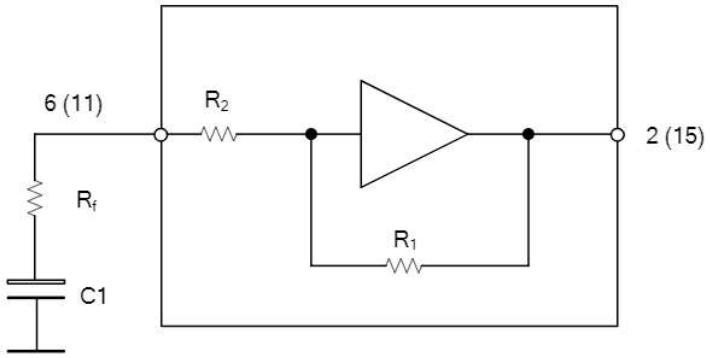


Figure 1

BRIDGE MODE (Figure 2)

The bridge configuration is realized very easily thanks to an internal voltage divider which provides (at pin 1) the CH 1 output signal after reduction. It is enough to connect pin 6 (inverting input of CH 2) with a capacitor to pin 1 and to connect to ground the pin 7.

The total gain of the bridge is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1}{R_f + R_2 + \frac{1}{JWC1}} \left(1 + \frac{R_3}{R_4} \frac{R_1}{R_2 + R_4 + \frac{1}{JWC1}}\right)$$

and with the suggested values (C1 = C2 = 100 uF, R_f = 0) means: Gv = 52 dB with first pole at f = 32 Hz

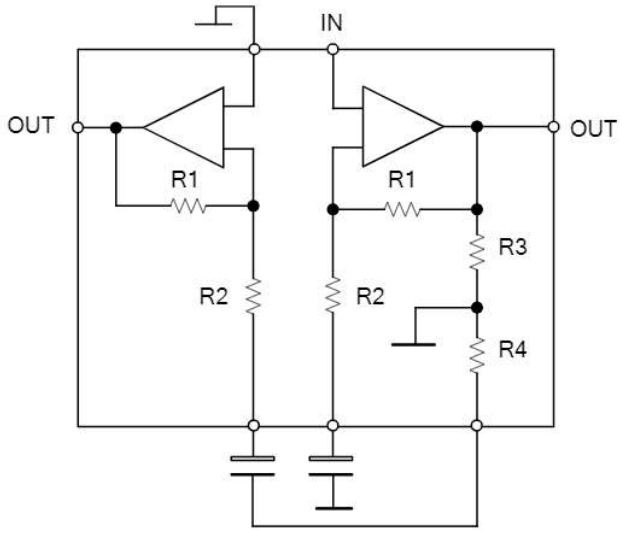


Figure 2

Output Capacitors

The low cut off frequency due to output capacitor depending on the load is given by:

$$F_L = \frac{1}{2\,\pi\,C_{OUT} \times R_L}$$

with C_{OUT} 470uF and R_L = 4 ohm it means F_L = 80Hz.

Pop Noise (Figure 3)

Most amplifiers similar to UTC **TEA2025** need external resistors between DC outputs and ground in order to optimize the pop on/off performance and crossover distortion.

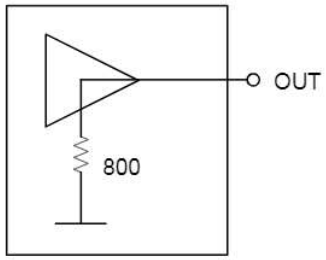


Figure 3

The UTC **TEA2025** solution allows to save components because of such resistors (800 ohm) are included into the chip.

Stability

A good layout is recommended in order to avoid oscillations. Generally the designer must pay attention on the following points:

- Short wires of components and short connections.
- No ground loops.
- Bypass of supply voltage with capacitors as nearest as possible to the supply I. C. pin. The low value (poliester) capacitors must have good temperature and frequency characteristics.
- No sockets.

The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_O (and therefore P_{tot}) and Id are reduced.

■ TYPICAL APPLICATION CIRCUIT

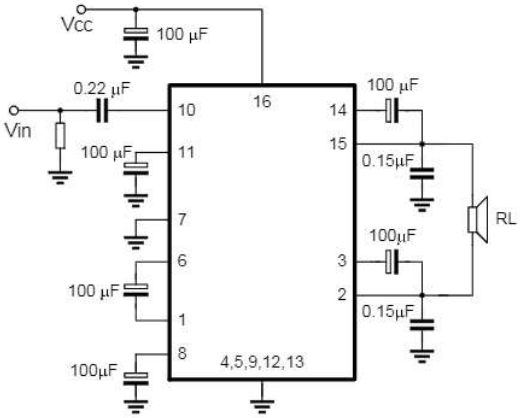


Fig. 4 Bridge Application

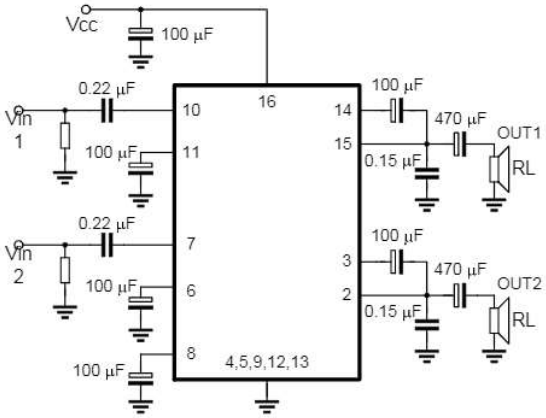
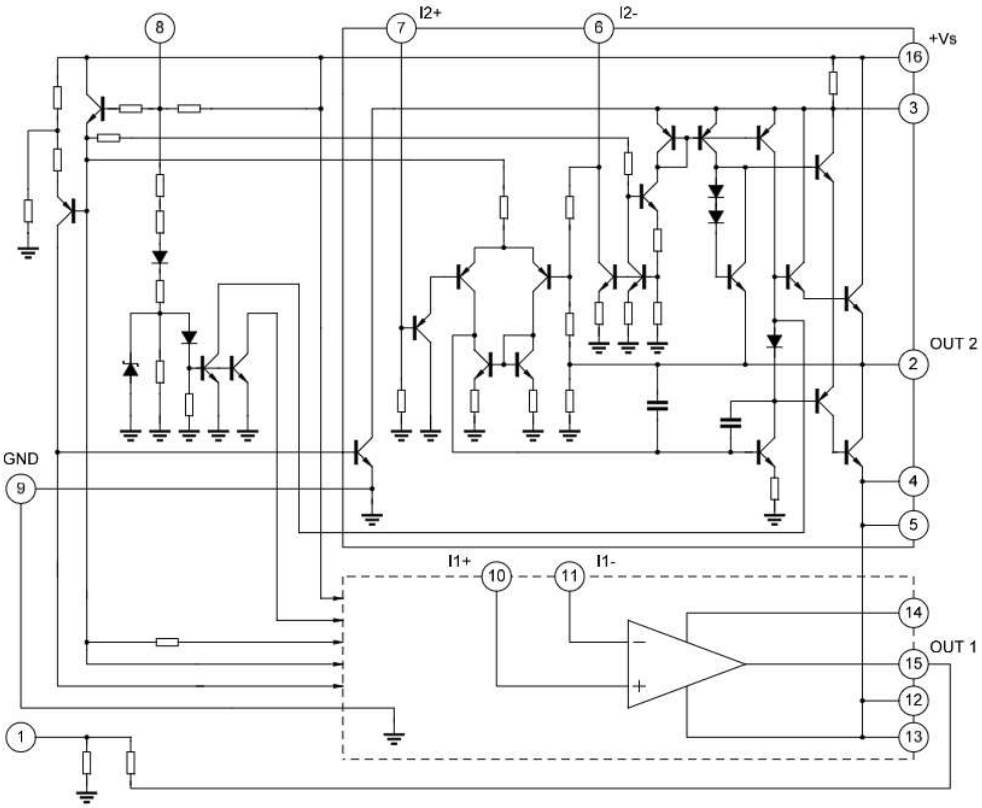


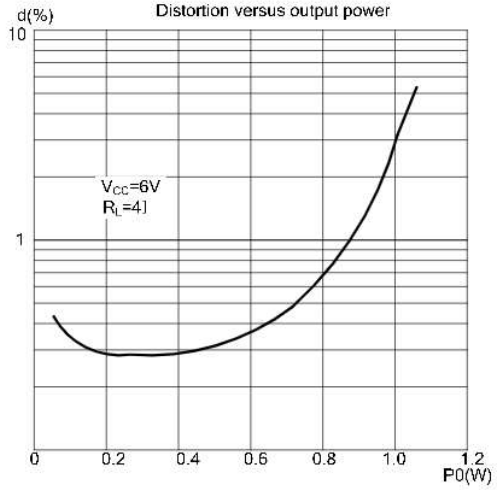
Fig.5 Stereo Application

■ SCHEMATIC DIAGRAM

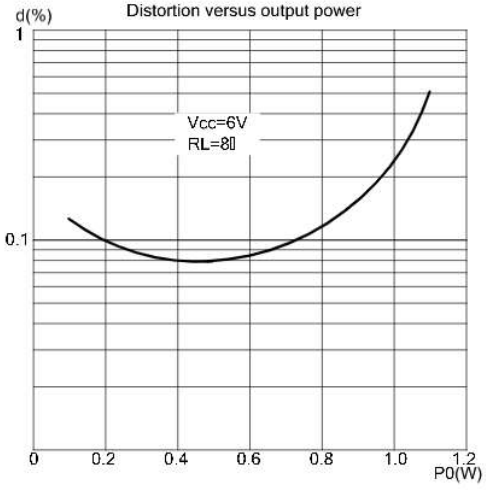


■ TYPICAL CHARACTERISTICS

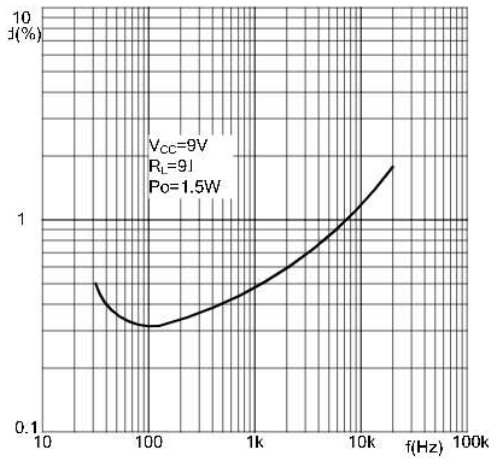
Distortion versus output power



Distortion versus output power



Distortion versus output Frequency



Output power/versus supply voltage